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ABSTRACT

Disclosed is a semiconductor integrated circuit realizing improved operating speed, reduced power consumption in an active mode, reduced power consumption in a standby mode, and reduced area of a chip. A first logic gate using a first pair of potentials VDDL, VSSL having a relatively small potential difference as an operation power source and a second logic gate using a second pair of potentials VDDH, VSSH having a relatively large potential difference as an operation power source commonly use substrate potentials VBP, VBN of MIS transistors. The second logic gate has a relatively high driving capability, and the first logic gate can operate on relatively low power. The MIS transistor has a threshold voltage which increases by a reverse substrate bias and decreases by a forward substrate bias. By commonly using the substrate potential, even in the case where different substrate bias states are generated at both of the logic gates, MOS transistors of the logic gates can be formed in the common well region.